IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant(s): | TANABE, et al. |
| Application No.: | TBD |
| Filed: | February 10, 2004 |
| For: | METHOD FOR FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE |
| Expected Group: | 2829 |
| Expected Examiner: | L. Kilday |

CLAIM FOR PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 10, 2004

Sir:

Pursuant to the requirements of 35 U.S.C. § 119 and 37 CFR § 1.55, Applicants respectfully claim priority based on Japanese Patent Application Serial No. 9/50781, filed in Japan on March 5, 1997.

As indicated in the Notification of Acceptance of Application Under 35 USC 371 and 37 CFR 1.494 or 1.495 mailed November 10, 1999 in Serial No. 09/380,646, filed September 7, 1999, the Priority Document for the above-identified Japanese Patent Application was received in prior application Serial No. 09/380,646.

Respectfully submitted,

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